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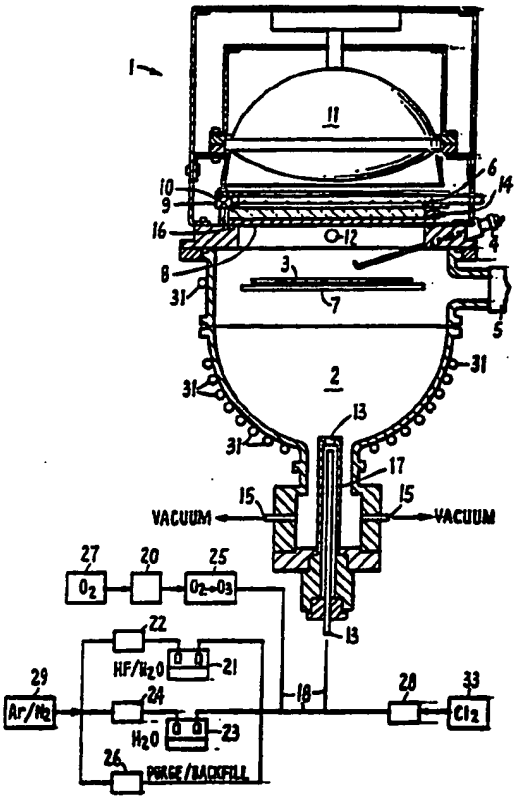
(54) Title: ORGANIC PRECLEAN FOR IMPROVING VAPOR PHASE WAFER ETCH UNIFORMITY

(57) Abstract

A method for achieving greater uniformity and control in vapor phase etching of silicon, silicon oxide layers and related materials associated with wafers used for semiconductor devices comprises the steps of first cleaning the wafer (3) surface to remove organics, followed by vapor phase etching. An integrated apparatus (1) for cleaning organic contamination and, subsequently, vapor phase etching, is also described.



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ORGANIC PRECLEAN FOR IMPROVING VAPOR PHASE WAFER ETCH UNIFORMITY

BACKGROUND OF THE INVENTION

This invention relates to a method for achieving greater uniformity and control in vapor phase etching of silicon, silicon oxide layers and related materials associated with wafers used for semiconductor devices, and an apparatus in which the method may be practiced.

Various combinations of oxygen, ozone, infrared (IR) and ultraviolet (UV) radiation have been studied as so-called "dry" process wafer cleaning methods. For example, Ruzyllo et al., "Preoxidation UV Treatment of Silicon Wafers", J. Electrochem. Soc., 134, 2052 (1987), reports the use of ozone in the presence of UV for the removal of carbon containing compounds prior to thermal growth of gate oxides. An earlier work Vig, "Ozone Cleaning of Surfaces", J. Vac. Sci. Tech., A3, 1027 (1985) reports the advantages of using an UV/ozone surface cleaning method, and the UV wavelengths most appropriately used for cleaning different types of materials from wafer surfaces.

Another paper, Zazzera et al., "XPS and SIMS Study of Anhydrous HF and UV/Ozone - Modified Silicon (100) Surfaces," J. Electrochem. Soc., 136, 484 (1989) studies, among other processes, UV/Ozone exposure as a post-HF etch for the removal of carbon containing compounds.

None of these papers, however, discusses the removal of carbon containing matter immediately prior to etching silicon or silicon oxide layers.

Vapor phase etching of silicon and silicon oxide layers has become more attractive for reasons including the use of smaller quantities of acidic

etchants, the speed with which etching occurs and the improved etching uniformity needed for effective removal of contaminants from submicron device features. With the decrease in feature size, the need for greater etch uniformity becomes paramount. Thus, it is an object of the invention to identify a method and apparatus by which greater etch uniformity and control can be achieved.

SUMMARY OF THE INVENTION

To achieve this object, the present invention comprises a method of removing organic contaminants from a wafer surface prior to exposing the wafer surface to vapor phase etchants. It has been found that the removal of organics prior to vapor phase etching of silicon, silicon oxide or related materials significantly improves etch uniformity.

In a preferred embodiment, the method comprises exposing a heated organic contaminated wafer to ozone to remove organic matter, followed by vapor phase HF/H_2O oxide or Cl_2/UV silicon etching.

In another aspect, the invention comprises an apparatus for carrying out both the "pre-etch" organic cleaning process and the subsequent vapor phase oxide or silicon etch, comprising a pressure controlled chamber for surrounding a wafer, the chamber having vapor inlet and outlet channels and an etchant resistant window for allowing UV and/or IR light to pass from outside the chamber to the surface of the wafer within the chamber. A preferred form of the apparatus utilizes a quartz/Teflon® window assembly.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be better understood by reference to the attached figures of which:

FIGURE 1 shows a cross-sectional view of the pressure chamber of the invention; and

FIGURE 2 is a enlarged view of the apparatus shown in FIGURE 1 showing an additional embodiment of the UV/IR transparent window assembly used therein.

DETAILED DESCRIPTION OF THE INVENTION

Silicon oxides, especially those formed thermally by the reaction of silicon with either oxygen (O_2) or water vapor (H_2O) at temperatures ranging from 800° to 1200°C, are critical in the fabrication of advanced integrated circuits. These oxides range in thickness from less than 100 Å (10 nm) to greater than 5000 Å (0.5 μm). Thermal oxide thicknesses are typically controlled by adjusting oxidation time and temperature. Uses of thermal oxides include gate dielectrics, field oxides, insulators and spacers, capacitors, and others.

In certain cases during device fabrication, thermal oxides must be etched back or removed completely in particular regions. This is generally accomplished by HF/H_2O solutions, sometimes with the addition of a NH_4F buffering agent for better control of pH and concentrations. In the case of vapor phase cleaning and etching technologies, HF/H_2O mixtures are also employed; however, no buffering agent is required. The typical chemistry involved in the etching of thermal oxide (SiO_2) with hydrofluoric acid (HF) follows the reaction:

$$4\ HF + SiO_2 \rightarrow SiF_4 + 2\ H_2O \qquad [1]$$

In addition to SiF_4 and H_2O which can be volatilized, various other intermediate species, such as H_2SiF_6, $Si(OH)_4$, and others may remain on the wafer

surface and must be removed. In the case of etching oxides part way to the silicon, these are generally not a problem.

While the present invention is directed to an improvement in the uniformity achieved with vapor phase etching, such etching does not form the invention in and of itself. Rather, the invention is a combination of process steps including an organic preclean in conjunction with, and prior to, such etching to achieve better uniformity.

An example of vapor phase HF/H_2O etching which can be used in the present invention is described in PCT application publication number WO 90/04045, published 19 April 1990, the contents of which are hereby incorporated by reference.

In the case of such vapor phase etching or cleaning, the mechanism has been found to involve two steps. The first is that the warm gas mixture being transported to the wafer condenses on the wafer surface - either oxide or silicon. The time required for condensation depends on several factors, including pressure, temperature difference between wafer and vapors, nature of the wafer surface, and concentration of the gas mixture (HF and H_2O for example). Typically, the condensation time (or "delay time") varies from no delay to more than 20 seconds.

As the condensed HF/H_2O layer increases in thickness up to tenths of micrometers or even micrometers, an equilibrium concentration is obtained, and etching of the oxide begins (second step). This etching is essentially identical to that occurring in conventional aqueous etching. At this point, etch rates are dependent only on the HF/H_2O layer concentration and the wafer temperature, not the gas pressure, wafer surface condition, etc. For

more dilute HF conditions, delay times are close to zero, while more concentrated HF (less H_2O) results in longer delay times. Once oxide etching begins, a linear relationship is obtained and etch rates can be specified.

While water is a reaction product of the HF/SiO_2 reaction (see Eq.[1]), water apparently must be present on the oxide surface before the reaction can proceed. Thus, anhydrous HF will not generally etch thermal oxide without the addition of H_2O.

Semiconductor wafer surfaces can become contaminated by a variety of organic compounds during wafer fabrication. Examples include photoresist, plasticizers from plastic boxes, human oils, cosmetics, paint fumes and other airborne organics. Such organics may collect on the surface of a wafer over a relatively brief period, for example over an hour or more, even under otherwise clean conditions.

Generally, the effects of surface organics on HF etch uniformity are not significant in conventional liquid HF silicon dioxide etching. This is because with immersion or spray HF etching wetting takes place quickly, and etching begins almost immediately. Since across wafer exposure to liquid etchants and water quenches is very quick relative to etch rates, uniformity is not a problem. Uniformity problems which do occur arise more from the method than from the organic contamination, as long as gross organics from photoresist or plasma have been removed.

Further, the sheer volume of etchant used in liquid etching provides a mechanism for the contaminants removed from the wafer surface to be carried away - again providing for relatively uniformly etched surfaces.

Because vapor phase cleaning occurs in two distinct processes materials which affect the

condensation rate will delay the time at which the actual etching portion of the process begins. Organics are believed to affect the vapor phase etching process in this way. Considering the relatively high rate of etching and the differences in the time at which condensation sufficient for etching occurs across the wafer, non-uniformities result.

In order to minimize these non-uniformities various methods of wafer treatment were studied as indicated in the following examples.

EXAMPLE 1

A pre-treatment for the removal of organics from wafer surfaces was developed to test the effect of organic removal on subsequent etch uniformity across wafer surfaces. Hexamethyl-di-silizane (HMDS), an organic primer, was deposited in thin layers on silicon wafers, and the pre-treatment indicated was applied. Analysis of the HMDS material was carried out before HMDS deposition, after deposition and after cleaning using static secondary ion mass spectrometry (SIMS).

Ten wafers were processed under the following conditions:

(1) Ozone produced using 4 liters/minute (LPM) O_2 feed to an ozone generator, the ozone then fed to the wafer surface in a pressure controlled chamber.
(2) UV at low power (corresponding to wafer temperature of about 225-250°C).
(3) Pressure of 300 Torr.
(4) Exposure time of 60 seconds.
(5) Wafer held horizontally in chamber.

The following results were obtained:

TABLE 1

WAFER	TYPE	HMDS/Si Ratio (2 spots/wafer)
1	Bare Si - Control	0.03, 0.02
2	HMDS - Control	0.91, 0.89
3	Processed	0.04, 0.03
4	Processed	0.03, 0.02
5	Processed	0.12, 0.09
6	Processed	0.03, 0.01
7	Processed	0.02, 0.02

These measurements were made using the 73 amu peak for $Si(CH_3)_3$ to ^{28}Si peak ratio. Additional samples were analyzed by a different lab with the following results:

TABLE 2

WAFER	TYPE	Normalized HMDS to Bare Silicon
1	Bare Si-Control	1.0
2	HMDS - Control	10.0
3	Processed	0.09
4	Processed	0.26
5	Processed	0.14
6	Processed	0.11
7	Processed	0.18
8	Processed Bare Wafer	0.16

These measurements were made using the 43 amu peak which includes the $SiCH_3$ fragment associated with HMDS, but can also include other compositions of the same mass. The data are normalized to the 43 amu peak for the bare Si control. As can be seen from Table 2 strong removal of HMDS is observed and even the processed bare silicon wafer (no. 8) is considerably cleaner than the bare silicon control (no. 1) and comparable to the HMDS cleaned wafers

(nos. 3-7). For the purpose of Table 2, the 43 amu peak was reduced by a factor of 6 on the bare silicon wafer.

These experiments indicate the ability to remove organics from wafer surfaces by application of ozone to heated wafer surfaces.

EXAMPLE 2

To test the effectiveness of alternative processes for hydrocarbon removal, an additional series of tests was run.

Eight HMDS contaminated wafers were processed in O_3/IR(UV), O_3/IR, and the N_2/IR(UV) processes for different lengths of time. The flows for both O_2 and N_2 were 4 SLPM, and process pressure was 500 Torr. Static SIMS analysis was performed. The results are listed below in the HMDS/Si peak ratios.

TABLE 3

Wafer ID	Process	HMDS/Si Ratio (two-point average)	Normalized to Bare
Wafer #1 Bare Wafer Control	None	0.02	1.0
Wafer #2 HMDS Control	None	0.79	40.0
Wafer #3 HMDS Wafer	N_2/IR(UV) 180 s	0.035	1.8
Wafer #4 HMDS Wafer	N_2/IR(UV) 180 s	0.02	1.0
Wafer #5 HMDS Wafer	O_3/IR(UV) 45 s	0.01	0.5
Wafer #6 HMDS Wafer	O_3/IR(UV) 100 s	0.03	1.5
Wafer #7 HMDS Wafer	O_3/IR(UV) 180 s	0.02	1.0
Wafer #8 HMDS Wafer	O_3/IR 180 s	0.015	0.8
Wafer #9 HMDS Wafer	O_3/IR 100 s	0.015	0.8
Wafer #10 HMDS Wafer	O_3/IR 45 s	0.01	0.5

Note: IR (UV) indicates the use of a radiation source including both IR and UV radiation. For wafers 3-10 radiation was used to heat the wafer to approx. 250°C.

As can be seen in Table 3, all processes tried were effective for removing HMDS. It is believed that HMDS is a relatively easy organic to remove, and other combinations of heat, ozone and time are likely required for other organics.

Example 3

Experiments were next carried out to determine the effect, if any, of organic removal from oxide surfaces on uniformity of oxide etching using azeotropic vapor phase HF/H_2O. Results are summarized in Table 4. In this experiment, approximately 1200Å of oxide were removed from wafers following various pre-treatments as indicated. It was observed quite clearly that all the pre-treatments improved oxide

etch uniformity, with No. 6 providing the lowest one-sigma value of 1.27%. This treatment involved 225-250°C heating with UV in N_2 and then an ozone treatment, with wafers held in a horizontal position.

TABLE 4

Wafer number	Description of Pre-Etch Treatments	Etch Time HF/H_2O	Etching Uniformity [Å unless noted] MEAN	1 σ [%]	1 σ	MIN	MAX
1	Control: No Pre-Treatment	50 sec.	1175.0	3.60%	42.3	1108	1237
2	2.0 Minutes UV + Ozone [Face-up]	50 sec.	1216.0	1.47%	17.8	1180	1244
3	2.0 Minutes UV + Ozone [Face-up]	50 sec.	1198.5	1.45%	17.4	1155	1223
4	2.0 Minutes UV + Oxygen [Face-up]	50 sec.	1199.9	2.01%	24.1	1152	1245
5	3.0 Minutes UV in N2, then 2.0 Minutes N2 soak [Face Down]	50 sec.	1178.5	1.57%	18.6	1124	1204
6	3.0 Minutes UV in N2, then 2.0 Minutes Ozone soak [Face Down]	50 sec.	1168.0	1.27%	14.8	1122	1194

COMMENTS [about etching inhibition], by wafer number:

1 Severe Pre-Etch contamination: ~3.8 cm
2 Some Pre-Etch contamination: Up to ~1.8 cm
3 Some Pre-Etch contamination: Up to ~1.3 cm
4 Some Pre-Etch contamination: Up to ~1.3 cm
5 Some Pre-Etch contamination: Up to ~1.3 cm
6 Cleanest Wafer [apparatus holder cooling effect seen at edge]

For pretreatment, 300 Torr pressure was used, UV at low power (225-250°C), and all etching occurred within 40 minutes of pretreatment. The etching process conditions were 125 Torr using 5.0 SLPM N_2, using

EXAMPLE 4

During testing of the present invention rooms adjacent to the lab in which wafers were located were painted. Paint fumes in the ambient were found to be responsible for severe degradation of oxide etch uniformity. To study this effect function wafers were purposely exposed to paint fumes. The results are shown in Table 5.

TABLE 5

Wafer number	Description of Pre-Etch Treatments	Etch Time	Etching Uniformity [Å unless noted]				
			MEAN	1 σ [%]	1 σ	MIN	MAX
1	CONTROL: Pre-treatment 24 hours before etch. Stored in plastic box	50 sec.	1208.8	4.56%	55.1	1123	1297
2	Same as WF#1, + 2nd O3 pre-treat, transport in clean qrtz elephant, immediately etched	50 sec.	1270.3	1.64%	20.8	1227	1316
3	Same as WF#1, + 2nd O3 pre-treat, exposed to latex paint fumes ambient for ~ 60 seconds, then etched	50 sec.	1217.3	2.86%	34.8	1118	1258
4	Same as WF#1, + 2nd O3 pre-treat, exposed to latex paint fumes ambient for ~ 300 seconds, then etched						
5	Same as WF#1, + 2nd)3 pre-treat, transport in clean qrtz elephant, stored in the elephant for ~ 5 minutes, then etched	50 sec.	1317.9	2.46%	32.5	1255	1377

COMMENTS [about etching inhibition]

1 Severe organic contamination effect seen
2 Very Clean. No visual evidence of any organic effect
3 Organic effect seen within ~2mm-10mm of wafer edge
4 Organic effect seen within ~5mm-20mm of wafer edge
5 No visual evidence of any organic effect

For pretreatment 300 Torr pressure was used, UV light source at high power (325-350°C) using 60 second ozone xposure at 4 SLPM O_2 flow into the ozone generator, all tching occurred within 5 minutes of pretreatment. Except where indicated, etching

process conditions were 125 Torr, 5.0 SLPM N_2 flow, using.

EXAMPLE 6

A series of 24 wafers were oxide etched after opening a new box of wafers. Every other wafer was subjected to UV (heat) and ozone pre-treatment. As can be seen in Table 6, the average one-sigma uniformity value for untreated wafers was 6.17%. For pre-treated wafers the average uniformity was 2.12%.

TABLE 6

Wafer number	Pretreatment	Amt of ox. etched	Difference 1 σ%
1	NO	459 Å	7.17
2	YES	392 Å	2.46
3	NO	472 Å	6.88
4	YES	428 Å	2.06
5	NO	474 Å	6.51
6	YES	432 Å	1.81
7	NO	482 Å	6.90
8	YES	431 Å	2.41
9	NO	489 Å	5.57
10	YES	427 Å	2.23
11	NO	489 Å	7.31
12	YES	446 Å	2.21
13	NO	487 Å	5.08
14	YES	432 Å	1.86
15	NO	483 Å	5.81
16	YES	475 Å	2.11
17	NO	505 Å	5.39
18	YES	426 Å	2.09
19	NO	485 Å	6.12
20	YES	441 Å	2.02
21	NO	481 Å	5.20
22	YES	430 Å	2.12
23	NO	496 Å	6.10
24	YES	433 Å	2.05

Pre-treat. Ave = 2.12% (1.81-2.46)
No Pre-treat. Ave = 6.17% (5.08-7.17)

EXAMPLE 7

4,000Å wafers were exposed in a Class 10 clean room for 16 hours prior to azeotropic HF/H_2O vapor phase etching. The three pre-treatment splits included (1) no additional treatment, (2) IR heating, and (3) UV/O_3 treatment in a UVOCS brand UV/ozone

tr atment chamber. The details of the process conditions are listed below.

Pretreatment process conditions for (2) and (3):

(2) IR Pre-treatment.

IR	4 SLPM O_2	300 Torr	120 sec

(3) UV/O_3 Pre-treatment.

UVOCS system	4 SLPM O_2	760 Torr	120 sec

Azeotropic Etch.

Frontside etch @	5 SLPM HF	125 Torr	22 sec

Azeotropic etch was done in the Advantage Production Technology Edge 2000 vertical vapor phase processing machine. The effect of the pre-treatments are listed in Table 7, which indicates that both the IR and UVOCS treatments substantially improved the etch uniformity. The IR pre-treatment gave better results than the UVOCS system. The averages of the standard deviations for the three conditions are

No Pre-treatment	$1\sigma = 4.1$
IR	$1\sigma = 1.2$
UVOCS	$1\sigma = 1.7$

TABLE 7

Wafer No.	Pretreatment	Amount Etched	Range	Std. Dev 1σ
1	None	663	153	4.0
2	IR	672	39	1.3
3	UVOCS	719	47	1.8
4	None	648	122	4.1
5	IR/O_2	686	23	0.97
6	UVOCS	702	59	2.1
7	None	693	137	3.9
8	IR	716	39	1.4
9	UVOCS	721	35	1.5
10	None	673	144	4.3
11	IR	734	25	1.0
12	UVOCS	774	45	1.4

In light of these data, it is clear that pretreatment of wafer surfaces to remove organics followed by vapor phase oxide etching results in significantly greater surface uniformity.

EXAMPLE 8

Silicon etch rates were measured on the same system as for Example 1, using an UV-Cl_2 ambient. Etch times of 60, 180, and 600 seconds were used. The wafers were substrates patterned with windows in a 5,500 Å thermal oxide. Some wafers were given a sequential UV-O_3 treatment prior to etching. The wafer surface was formed by opening windows in the thermal oxide with an HF strip, and then removing the resist used to define the windows. A final wet H_2SO_4:H_2O_2 clean was used to remove the residual photoresist residues.

The chlorine/UV etch rates delay times for these surfaces were:

Substrate	Delay Time	Etch Rate
Untreated	140 sec	23.2 Å/sec
UV-O_3 Pretreatment	30 sec	52.6 Å/sec

The longer initiation (delay) time found for the wafers not pretreated is likely due to hydrocarbon contamination on the surface that would be removed by the UV-O_3 pretreatment. The hydrocarbon layer on the untreated surface probably becomes modified by the UV-Cl_2 etch, however, its influence continues to affect the etch process, as indicated by the reduced etch rate for the untreated wafers. The masking effect could be due to formation of a very stable silicon carbide layer on the surface of the untreated wafers.

We have found that in addition to improving uniformity for Cl_2/UV etching, the organic pre-clean step of the invention shortens the delay time and increases the etch rate. It also minimizes surface roughness on the wafer.

APPARATUS

In light of these findings, a device in which the process of the invention may advantageously be carried out is shown in Figures 1 and 2. Depending on the type of wafer handling system with which the apparatus is used, apparatus 1 may be adapted to hold the wafer either vertically or horizontally. In the system as shown, a pressure controlled chamber 2 is shown in cross-section. Within chamber 2, wafer 3 is supported by wafer support ring 7, and enters/exits chamber 2 via access port 5, using a wafer transport mechanism (not shown). Support ring 7 supports wafer 3 around the edges of the wafer such that both faces of wafer 3 are exposed to the atmosphere within the

chamber and either backside or frontside etching may be used.

Sealing one end of chamber 2 is window assembly 9. Radiation source 11, such as a UV and/or IR light source, is positioned adjacent window assembly 9 such that when source 11 is operating, radiation will pass through window 9 and heat wafer 3. A number of interchangeable bulbs are available to serve as radiation source 11, depending on the wavelength desired. Any such bulb is suitable which provides the ability, in conjunction with window assembly 9, to heat the wafer surface for organic cleaning and which provides UV in the appropriate 300-400 nm wavelength necessary to form Cl^- from chlorine where chlorine etching is desired. In the experiments described above, a Fusion brand PL-150 Illuminator UV/IR source, among others, was used. Where heating alone is desired, IR in the wavelength 0.8 to 1.2 micrometers may be used.

As is known from PCT application publication WO 90/04045, the desired etchants are supplied via heated vapor lines 18 to inlet port 13. For ozone pre-cleaning, oxygen from oxygen source 27 is passed through mass flow meter 20 to ozone generator 25. Valves within the vapor supply system, as well as pumps and the like, are not shown. Argon and/or nitrogen from source 29 may be used to carry vapor from vaporizers 21 and 23 through mass flow meters 22 and 24 for HF oxide etching. Further, argon and/or nitrogen may be pumped through mass flow meter 26 to purge or backfill the system, as desired.

Alternatively, a source of chlorine 33 may be pumped through mass flow meter 28 for chlorine etching. Vapors exit the chamber through vaccuum ports 15.

Chamber 2 will be h ated by use of radiation s urce 11, and chamber walls are cooled externally by circulating water through cooling coils 31. Window assembly 9 is cooled by annular cooling ring 6, external to chamber 2. Cooling ring 6 supplies chilled clean air through orifices 30 equally distributed around the window. When desired, wafer 3 can also be cooled by use of cool gas, such as CO_2, passing through tube 12, and into chamber 2. Thermocouple 4 is used to monitor and track the temperature of wafer 3 within chamber 2.

An important element of the apparatus is window assembly 9. Assembly 9 comprises upper window 10, and lower window 8. A two window assembly is used to assure strength and to allow lower window 8 to be formed from a corrosion resistant material. Highly corrosive materials such as HF vapor used for wafer etching require the use of a window material which will not degrade. Additionally, any material used in window assembly 9 must necessarily allow the desired UV and IR wavelengths to pass.

We have found it is most desirable to use as lower window 8 an amorphous copolymer material described in detail in U.S. Patent No. 4,754,009, the entire disclosure of which is incorporated herein by reference, which material is sold under the trademark Teflon® AF by DuPont Polymer Products Department, Wilmington, Delaware. This material exhibits the necessary stability and radiation passing characteristics required in the present apparatus and process. A window thickness of about ¼ inch is preferred. As upper window 10, a ½ inch thick fused quartz available from General Electrics quartz products division (GE124), about 7½ inches in diameter is preferred. Dynasil 5000 synthetic fused quartz can also be used.

Positioned adjacent window assembly 9 at the interface between windows 8 and 10, is vacuum nozzle 14, through which a vacuum may be applied between windows 8 and 10. This assures that any gasses are drawn from the window assembly which might affect the performance of the apparatus. While it is preferred to use this two window assembly, it is also possible to use a one window assembly under certain process conditions, where that window is sufficiently resistant to corrosive etchants. Window assembly 9 is sealed in the apparatus using "O"-ring seal 16.

An alternative window arrangement which has been found to work satisfactorily in the invention is shown in Figure 2. Figure 2 is an enlarged view of a portion of the apparatus of Figure 1. The elements of Figure 2 are in all respects the same as Figure 1 with the exception of window assembly 9. In Figure 2, window assembly 9 now comprises a quartz window, optimally about ½ inch thick having a layer 8A of FEP (fluorinated ethylene propylene) polymer 2 mils thick surrounding the quartz for protection from HF, chlorine and the like. Teflon® FEP resin which is preferably used (available from DuPont Polymers) is a copolymer of tetrafluoroethylene and hexafluoropropylene having the formula $[CF(CF_3) - CF_2(CF_2-CF_2)_n]_m$. It is preferred that layer 8A of the resin be from about 2 mil to about 5 mil in thickness. It has been found that the film is most advantageously put in place around the optical grade quartz window (Dynasil 5000 synthetic fused quartz brand window or GE124, about ½ inch thick) by thermal wrapping, which wrap can be accomplished by American Durafilm.

In the process of the invention, using apparatus 1 of Figures 1 and 2, the organic pre-clean and subsequent silicon or oxide etch can now take place

in a single unit to achieve improvements in overall etch uniformity. In addition, decreases in the vapor phase etch delay time, increases in the rate of etching, and reduced surface roughness are achieved for etching silicon.

While the preferred apparatus and method have been described, other embodiments which achieve the same function as recognized by those skilled in the art are intended to be encompassed in the appended claims. For example, it is within the scope of the invention to utilize a conventional resistance heater to heat the wafer and simply use the appropriate UV wavelengths for chlorine etching, i.e., without using any infrared for heating. In such an instance, the integrated apparatus including the appropriate window assembly is still used to great advantage.

What is claimed is:

1. A method of etching silicon oxides from semiconductor wafer surfaces comprising the steps of:

(a) exposing an organic contaminated surface of a semiconductor wafer to ozone at a temperature of from 200°-400°C and a pressure of from 300-500 Torr for from 45-120 seconds to remove substantially all of said organic; and, subsequently

(b) exposing said surface cleaned of organic to HF/H_2O vapor to etch silicon oxide from said surface.

2. A method of etching materials from semiconductor wafers comprising the steps of:

(a) exposing an organic contaminated surface of a semiconductor wafer also carrying materials to be etched to conditions sufficient to remove substantially all of said organic from at least a portion of said surface; and, subsequently

(b) exposing said surface cleaned of organic to a vapor phase etchant to etch said materials from said wafer surface.

3. A method as in claim 2 wherein said material is silicon and wherein said step of exposing said surface cleaned of organic comprises the step of exposing said surface to UV excited chlorine.

4. A method as in claim 2 wherein said material is silicon oxide ands wherein said step of exposing said surface cleaned of organic comprises the step of exposing said surface to HF/H_2O vapor.

5. The method of claim 2 wherein each of said steps takes place in the same apparatus.

6. An integrated vapor phase etching apparatus comprising:

chamber means for containing a semiconductor wafer under a controllable pressure, said chamber means having a vapor inlet and a vapor outlet;

window means in a wall of said chamber, said window means comprising a sheet of polytetrafluoroethylene resistant to vapor phase chlorine and vapor phase hydrogen fluoride and water mixtures;

wafer support means in said chamber for supporting a wafer;

heating means for heating a surface of said wafer;

a source of ultraviolet light positioned outside said chamber and along a path such that, when activated, said ultraviolet light shines through said window and into said chamber.

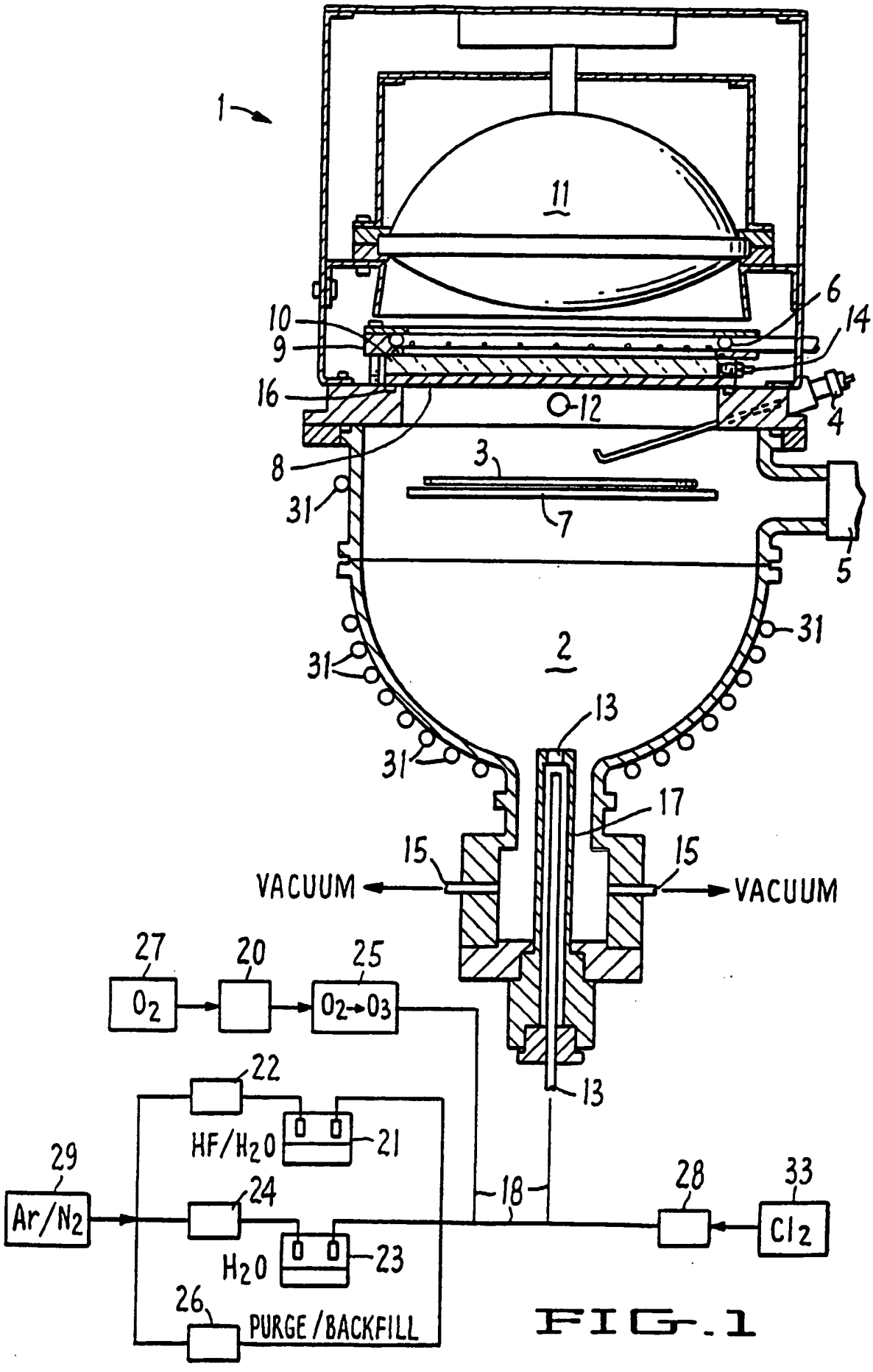
7. An apparatus as in claim 6, wherein said heating means comprises an infrared lamp positioned outside said chamber and adjacent said window in a position such that, when activated, radiation from said lamp passes through said window and irradiates a surface of said wafer.

8. An apparatus as in claim 6 where said sheet of polytetrafluoroethylene is an amorphous polymer in the form of a sheet approximately one half inch thick.

9. An apparatus as in claim 6 where said sheet of polyt trafluoroethylene comprises a film of

from about 2 to about 5 mils thick heat wrapped around a quartz window.

(1/2)


1
11
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16
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31
7
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2
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17
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VACUUM
27
20
25
O_2
$O_2 \rightarrow O_3$
22
HF/H_2O
21
29
Ar/N_2
24
18
28
33
Cl_2
H_2O
23
26
PURGE/BACKFILL

FIG. 1

(2/2)

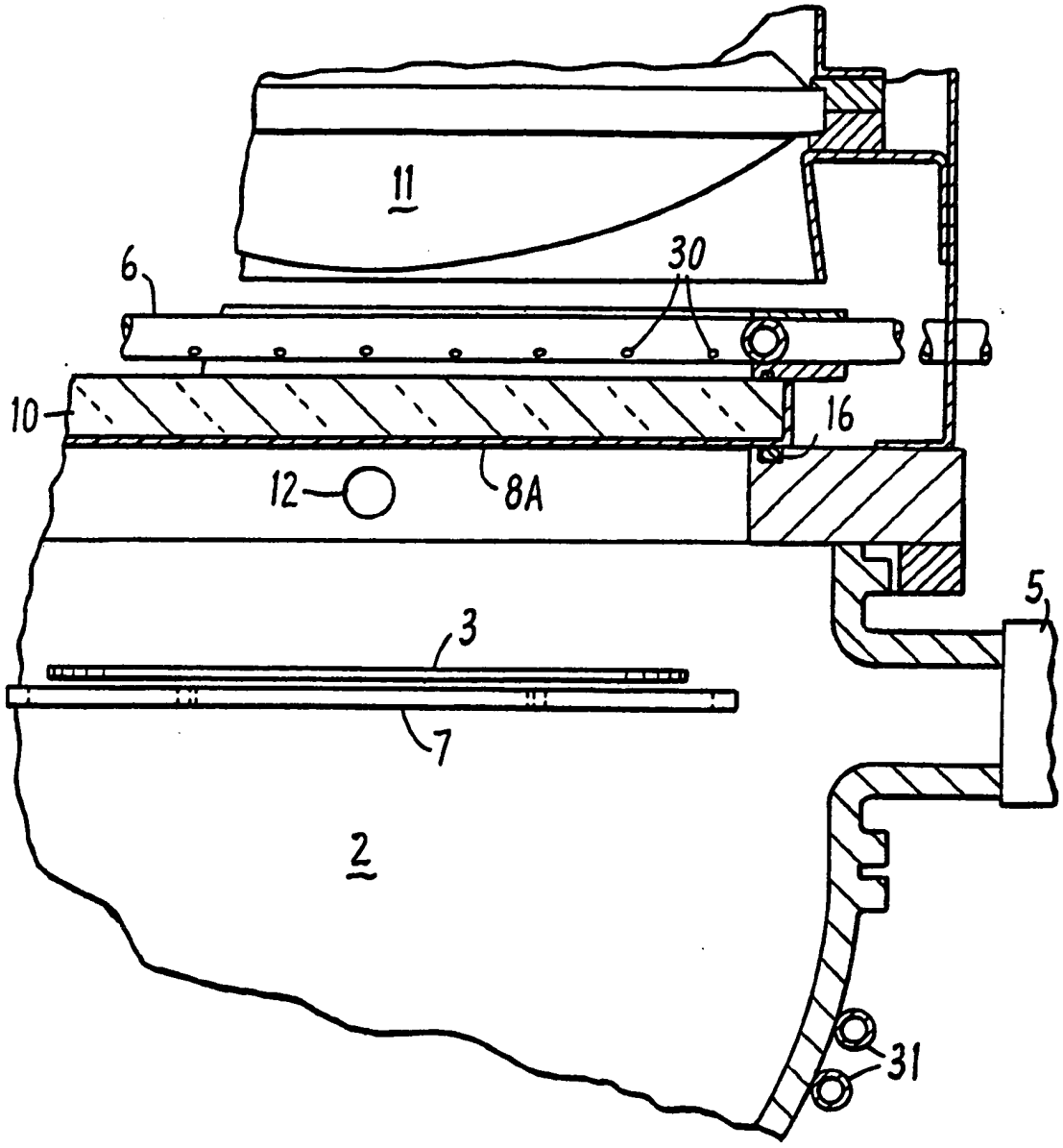

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/04175

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 21/00
US CL :156/643,646,662,668,651,652,653,345; 118/715,722
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. :

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,749,440 (BLACKWOOD ET AL.) 07 June 1988, See col. 1-col. 2.	1-5
Y	US, A, 4,906,328 (FREEMAN ET AL.) 06 March 1990, See col. 25-26.	1-5
A,P	US, A, 5,073,232 (OHMI ET AL.) 17 December 1991, See col. 2-3.	1-5
Y,P	US, A, 5,078,832 (TANAKA) 07 January 1992, See col. 20-22.	1-5
Y	US, A, 4,885,047 (URY ET AL.) 05 December 1989, See col. 5-8.	1-5
Y	JP, A, 02-010,726 (SUGINO) 16 January 1990, See Abstract.	1-5
Y	JP, A, 01 -217,921 (URISU ET AL.) 31 August 1989, See Abstract.	1-5

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 07 OCTOBER 1992	Date of mailing of the international search report 10 NOV 1992
Name and mailing address of the ISA/ Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer GEORGE A. GOUDREAU Telephone No. (703) 308-1915

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/04175

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation f document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	Applied Physics A, 1987, BAUMGARTNER ET AL., Ozone Cleaning of the Si-SiO_2 System, page 223.	1-5
Y	Journal of Applied Physics, 01 October 1988, The Formation of Hydrogen Passivated Silicon Single-Crystal Surfaces Using Ultraviolet Cleaning and HF Etching, page 3516.	1-5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/04175

B. FIELDS SEARCHED

Electronic data bases consulted (Name of data base and where practicable terms used):

APS; Orbit: WPAT, Japio, Inspec; STN: Ca

Ozone; organic; UV or ultraviolet; cl or chlorine;

HF or hydrofluoric acid; etch; SiO or silicon (w)(oxide or monoxide or dioxide)